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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/909,181	07/19/2001	Paul A. Farrar	MICRON.170A	9085

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[REDACTED] EXAMINER

CHU, CHRIS C

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 01/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	09/909,181	FARRAR, PAUL A. <i>Von</i>
	Examiner	Art Unit
	Chris C. Chu	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) Responsive to communication(s) filed on 11 October 2002.

2a) This action is **FINAL**.      2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4) Claim(s) 1 - 26 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 1 - 26 is/are rejected.

7) Claim(s) \_\_\_\_\_ is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on 11 October 2002 is: a) approved b) disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some \* c) None of:

1. Certified copies of the priority documents have been received.

2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.

3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ .
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .	6) <input type="checkbox"/> Other: _____

## **DETAILED ACTION**

### *Response to Amendment*

1. Applicant's amendment filed on October 11, 2002 has been received and entered in the case.

### *Drawings*

2. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on October 11, 2002 have been disapproved because they introduce new matter into the drawings. 37 CFR 1.121(a)(6) states that no amendment may introduce new matter into the disclosure of an application. The original disclosure does not support the showing of a fourth insulating layer being formed on the lower surface of the first chip.

3. Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect may be deferred until after the examiner has considered the proposed drawing correction. Failure to timely submit the proposed drawing correction will result in the abandonment of the application.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1 ~ 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asada in view of Morinaga.

Regarding claim 1, Asada discloses in Fig. 8B a high density semiconductor structure having a plurality of integrated circuit chips, comprising:

- a first integrated circuit chip (131) having an upper bonding surface;
- a second integrated circuit chip (132) secured to the first chip in a manner such that a lower bonding surface of the second chip is positioned adjacent to the upper bonding surface of the first chip; and
- a chip insulating layer (601) disposed between the first and second chips so as to provide electrical isolation between the chips, wherein the chip insulating layer comprises an insulating material.

Asada does not disclose the chip insulating layer comprising a plurality of enclosed regions of air dispersed throughout the insulating material, wherein the dielectric constant of the chip insulating layer is less than the dielectric constant of the insulating material. However, Morinaga discloses in Fig. 5 a chip insulating layer (502) comprising a plurality of enclosed

regions of air (505) dispersed throughout an insulating material, wherein the dielectric constant of the chip insulating layer is less than the dielectric constant of the insulating material. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Asada by using the plurality of enclosed regions of air into the chip insulating layer as taught by Morinaga. The ordinary artisan would have been motivated to modify Asada in the manner described above for at least the purpose of providing holes in the insulating layer (column 1, lines 32 and 33).

Regarding claim 2, Asada discloses in Fig. 8B a conductor insulating layer (621) formed on the upper bonding surface of the first chip, wherein the conductor insulating layer provides electrical isolation between adjacent conductive leads (611a and 611j) disposed on the upper bonding surface of the first chip, wherein the conductor insulating layer comprises an insulating material.

Asada does not disclose the conductor insulating layer comprising a plurality of enclosed regions of air dispersed throughout the insulating material, wherein the dielectric constant of the chip insulating layer is less than the dielectric constant of the insulating material. However, Morinaga discloses in Fig. 5 a plurality of enclosed regions of air (505) dispersed throughout an insulating material, wherein the dielectric constant of the chip insulating layer is less than the dielectric constant of the insulating material. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Asada by using the plurality of enclosed regions of air into the conductor insulating layer as taught by Morinaga. The ordinary artisan would have been motivated to modify Asada in the manner described above for at least the purpose of providing holes in the insulating layer (column 1, lines 32 and 33).

Regarding claims 3 and 4, Asada discloses in column 6, lines 47 ~ 51 the chip insulating layer comprising a foamed polymeric material.

Regarding claim 5, Asada discloses in column 6, lines 47 ~ 51 the foamed polymeric material comprising a foamed polyimide.

Regarding claim 6, Asada discloses the claimed invention except for the foamed polyimide being approximately 2.1 microns thick. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use approximately 2.1 microns thick for the foamed polyimide, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. The ordinary artisan would have been motivated to modify Asada in the manner described above for at least the purpose of decreasing the device height.

Regarding claim 7, Asada discloses the claimed invention except for the foamed polymeric material comprising a hydrophobic material wherein the hydrophobic material is treated so as to provide the material with hydrophilic properties. However, it is well known in the art to use hydrophobic material for polymeric material. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use hydrophobic material for polymeric material, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416. The ordinary artisan would have been motivated to modify Asada in the manner described above for at least the purpose of decreasing wiring capacity.

Regarding claim 8, Asada discloses the claimed invention except for the foamed polymeric material comprising polynorbornene. However, it is well known in the art to use polynorbornene for polymeric material. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use polynorbornene for polymeric material, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416. The ordinary artisan would have been motivated to modify Asada in the manner described above for at least the purpose of increasing speed of operation.

Regarding claims 9 and 10, Asada discloses the claimed invention except for each enclosed region of air being approximately 0.1 micron. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use approximately 0.1 micron for each enclosed region of air, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. The ordinary artisan would have been motivated to modify Asada in the manner described above for at least the purpose of decreasing the device height.

Regarding claim 11, Asada discloses in Fig. 8B each enclosed region of air being less than the minimum distance separating adjacent conductive leads.

Regarding claim 12, Asada discloses the claimed invention except for the dielectric constant of the chip insulating layer being approximately one third of the dielectric constant of the insulating material. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use approximately one third of the dielectric constant of the

insulating material to be the dielectric constant of the chip insulating layer, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. The ordinary artisan would have been motivated to modify Asada in the manner described above for at least the purpose of increasing operation speed.

Regarding claim 13, Asada discloses the claimed invention except for the dielectric constant of the insulating layer being less than 1.5. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use less than 1.5 dielectric constant for the insulating layer, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. The ordinary artisan would have been motivated to modify Asada in the manner described above for at least the purpose of increasing operation speed.

Regarding claim 14, Asada discloses the claimed invention except for the conductive leads being made of an aluminum alloy. However, it is well known in the art to use aluminum alloy for the conductive leads. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use aluminum alloy for the conductive leads, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416. The ordinary artisan would have been motivated to modify Asada in the manner described above for at least the purpose of increasing corrosion-resistant.

§

Regarding claim 15, Asada discloses in Fig. 8B a third integrated circuit chip (133) wherein the third chip is secured to the second chip in a manner such that a lower surface of the third chip is positioned adjacent an upper surface of the second chip wherein a third insulating layer (602) is disposed between the second and third chips.

Regarding claim 16, Asada discloses in column 6, lines 47 ~ 51 the third insulating layer comprising a foamed polymeric material.

Regarding claim 17, Asada discloses in Fig. 8B the first integrated circuit chip further comprising a lower surface wherein a fourth insulating layer (16) is formed on the lower surface of the first chip.

Regarding claim 18, since Asada does not limit the fourth insulating layer to any particular or specific material, hence his/her disclosure encompasses all well known material including “foamed polymeric material.”

Regarding claim 19, Asada discloses in Fig. 8B a multichip cube structure having a plurality of integrated circuit chips, comprising:

- a first integrated circuit chip (131) having a first insulating layer (621) disposed on an upper surface of the chip so as to electrically isolate a plurality of metal leads disposed on the upper surface thereof, wherein the first insulating layer is comprised of an insulating material having a first dielectric constant;
- a second integrated circuit chip (132) secured to the first chip in a manner such that a lower surface of the second chip is positioned adjacent the upper surface of the first chip;

- a second insulating layer (601) disposed between the first and second chips wherein the second insulating layer is comprised of a second insulating material having a second dielectric constant.

Asada does not disclose at least a portion of the first and second insulating layers containing a plurality of enclosed regions of air, the dielectric constant of the first insulating layer being lower than the first dielectric constant and the dielectric constant of the second insulating layer being lower than the second dielectric constant. However, Morinaga discloses in Fig. 5 at least a portion of the first and second insulating layers (502) containing enclosed regions of air (505), the dielectric constant of the first insulating layer being lower than the first dielectric constant and the dielectric constant of the second insulating layer being lower than the second dielectric constant. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Asada by using the enclosed regions of air as taught by Morinaga. The ordinary artisan would have been motivated to modify Asada in the manner described above for at least the purpose of providing holes in the insulating layer (column 1, lines 32 and 33).

Regarding claim 20, Asada discloses in column 13, lines 30 ~ 46 the first insulation material comprising a polymeric material.

Regarding claim 21, the limitation “the polymeric material is treated with a supercritical fluid so as to produce the enclosed regions of the air in the material” is product-by-process claim, even though product-by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious

from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A “product by process” claim is directed to the product per se, no matter how actually made, *In re Hirao*, **190 USPQ 15 at 17** (footnote 3). See also *In re Brown*, **173 USPQ 685**; *In re Luck*, **177 USPQ 523**; *In re Fessmann*, **180 USPQ 324**; *In re Avery*, **186 USPQ 116**; *In re Wertheim*, **191 USPQ 90** (**209 USPQ 254** does not deal with this issue); and *In re Marosi et al.*, **218 USPQ 289** final product per se which must be determined in a “product by, all of” claim, and not the patentability of the process, and that an old or obvious product, whether claimed in “product by process” claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 22, Asada discloses in Fig. 8B each enclosed region of air being less than the distance between adjacent metal leads on the upper surface of the first chip.

Regarding claim 23, Asada discloses in column 6, lines 47 ~ 51 the second insulating material comprising a polymeric material.

Regarding claim 24, Asada discloses in column 6, lines 47 ~ 51 the polymeric material being polyimide.

Regarding claim 25, Asada discloses the claimed invention except for the foamed polymeric material comprising polynorbornene. However, it is well known in the art to use polynorbornene for polymeric material. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use polynorbornene for polymeric material, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*,

125 USPQ 416. The ordinary artisan would have been motivated to modify Asada in the manner described above for at least the purpose of increasing speed of operation.

Regarding claim 26, the limitation “the insulating material is treated with a hydrogen containing radical so as to make the surface more hydrophilic” is product-by-process claim, even though product-by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A “product by process” claim is directed to the product per se, no matter how actually made, *In re Hirao*, **190 USPQ 15 at 17** (footnote 3). See also *In re Brown*, **173 USPQ 685**; *In re Luck*, **177 USPQ 523**; *In re Fessmann*, **180 USPQ 324**; *In re Avery*, **186 USPQ 116**; *In re Wertheim*, **191 USPQ 90** (**209 USPQ 254** does not deal with this issue); and *In re Marosi et al.*, **218 USPQ 289** final product per se which must be determined in a “product by, all of” claim, and not the patentability of the process, and that an old or obvious product, whether claimed in “product by process” claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

*Response to Arguments*

6. Applicant's arguments filed on October 11, 2002 have been fully considered but they are not persuasive.

On page 4, applicant argues “[A]pplicant notes that neither reference teaches or suggests a multichip module having an insulating layer comprised of enclosed regions of air.” This argument is not persuasive. In common knowledge, when layers cover empty holes without filling materials in the holes, the holes contain air. Since Morinaga’s enclosed regions (505) are empty holes, the holes (505) contain air. Therefore, Morinaga discloses an insulating layer (502) comprised of enclosed regions of air (505).

Further, in response to applicant's argument that there would have been no motivation to combine Asada with Morinaga to form a multichip module having an inter-chip insulating layer with enclosed regions of air dispersed therethrough to reduce capacitive coupling between conductors on adjacent chips, the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

Furthermore, applicant argues “Asada does not at all address the problem associated with capacitive coupling between conductors formed in adjacent chips.” This argument is not persuasive because it is noted that the features upon which applicant relies (i.e., capacitive coupling between conductors formed in adjacent chips) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Even further, applicant argues “[T]he formation of voids in the insulating substrate is likely to cause the copper wiring to delaminate from the insulating substrate in regions where the voids are present in the interface between the insulating substrate and the metal wiring, which can ultimately cause the module to malfunction.” This argument is not persuasive because the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

Finally, in response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). Contrary to applicant's assertion and as stated in previous rejection which is mailed on October 11, 2002, motivation was established by Morinaga, specifically in column 1 lines 32 and 33 (providing holes in the insulating layer).

For the above reasons the rejection is maintained.

*Conclusion*

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7382 for regular communications and (703) 308-7722 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu  
Examiner  
Art Unit 2815

c.c.  
January 9, 2003



CHRISS C. CHU  
EXAMINER  
ART UNIT 2815  
JANUARY 9, 2003